ABSTRACT OF THE DISCLOSURE

An apparatus for invalidating redundant entries in an N-way set associative branch target address cache (BTAC) for the same branch instruction is disclosed. An index portion of an instruction cache fetch address is applied to the BTAC to select a set of N ways therein. Control logic detects a condition in which more than one of the N ways of the selected set has a valid tag that matches the tag portion of the fetch address. A flag is set to indicate the occurrence of the condition, and the fetch address is stored in a register. The control logic subsequently invalidates all but one of the N ways having a valid tag that matches the fetch address tag.